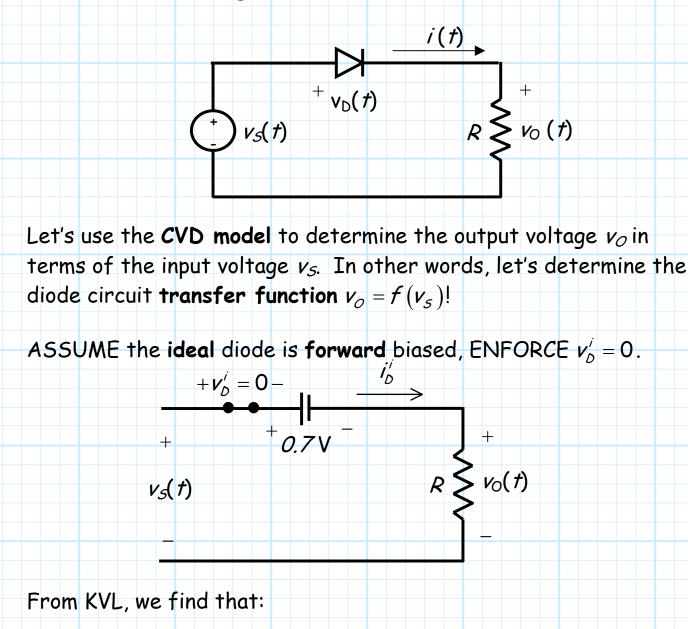
Example: Diode Circuit Transfer Function

Consider the following circuit, called a half-wave rectifier:



$$v_{\mathcal{O}}(t) = v_{\mathcal{S}}(t) - 0.7$$

This result is of course true **if** our original assumption is correct it is valid **if** the ideal diode is forward biased (i.e., $i_D^{\prime} > 0$)!

From Ohm's Law, we find that:

$$i'_{D} = \frac{v_{O}}{R} = \frac{v_{S} - 0.7}{R}$$

Q: I'm so confused! Is this current greater than zero or less than zero? Is our assumption correct? How can we tel!?

A: The ideal diode current is **dependent** on the value of source voltage $v_s(t)$. As such, we **cannot** determine **if** our assumption is correct, we **instead** must find out **when** our assumption is correct!

In other words, we know that the forward bias assumption is correct when $i_{D}^{i} > 0$. We can rearrage our diode current expression to determine for what values of source voltage $v_{S}(t)$ this is true:

$$i_{D}^{i'} > 0$$

$$\frac{v_{s}(t) - 0.7}{R} > 0$$

$$v_{s}(t) - 0.7 > 0$$

$$v_{s}(t) > 0.7$$

So, we have found that when the source voltage $v_{s}(t)$ is greater than 0.7 V, the output voltage $v_{c}(t)$ is:

 $\mathbf{v}_{\mathcal{O}}\left(t\right) = \mathbf{v}_{\mathcal{S}}\left(t\right) - 0.7$

Q: OK, I've got this result written down. However, I still don't know what the output voltage $v_O(t)$ is **when** the source voltage $v_5(t)$ is **less** than 0.7V!?!

Now we **change** our assumption and ASSSUME the ideal diode in the CVD model is **reverse** biased, an assumption ENFORCEd with the condition that $i'_{D} = 0$ (i.e., an open circuit).

 $i_{D}^{i} = 0$ $+V'_{D}$ -+ 0.7V + • *v*₀(*t*) v₅(†)

Q: Fascinating! The output voltage is **zero** when the ideal diode is reverse biased. But, precisely when **is** the ideal diode reverse biased? For **what** values of v₅ does this occur ?

From Ohm's Law, we find that the output voltage is:

$$v_{\mathcal{O}} = R i_{\mathcal{D}}^{i}$$
$$= R (0)$$
$$= 0 V \parallel \parallel$$

A: To answer these questions, we must determine the ideal diode voltage in terms of
$$v_s$$
 (i.e., $v'_b = f(v_s)$):
From KVL: $v_s - v'_b - 0.7 = v_o$
Therefore:
 $v'_b = v_s - 0.7 - v_o$
 $= v_s - 0.7 - 0.0$
 $= v_s - 0.7 - 0.0$
 $= v_s - 0.7$
Thus, the ideal diode is in reverse bias when:
 $v'_b < 0$
 $v_s - 0.7 < 0$
Solving for v_s , we find:
 $v_s - 0.7 < 0$
 $v_s < 0.7 V$
In other words, we have determined that the ideal diode will be reverse biased when $v_s < 0.7 V$, and that the output voltage will be $v_o = 0$.
Q: So, we have found that:
 $v_o = v_s - 0.7 V$
In other $v_s < 0.7 V$, and that the output voltage will be reverse biased when $v_s < 0.7 V$.
In other $v_s < 0.$

